2.1 A Fully Integrated 4×10Gb/s DWDM Optoelectronic Transceiver in a standard 0.13µm CMOS SOI

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The integration of optical functions with CMOS electronics provides a low-cost scalable solution for high-bandwidth fiber-optic links. Recent advances in SOI photonics have enabled the transmission and reception of 10Gb/s on a single optical wavelength [1]. DWDM allows a single strand of single mode fiber to carry many such streams of data over different wavelengths, allowing for higher data rates and reaches that are inaccessible to copper solutions limited by signal attenuation, dispersion, and cross-talk [2, 3]. DWDM systems are already extensively used in long-haul telecom. However, such systems consist of large racks of extremely expensive equipment. The integration of an entire 4-wavelength DWDM transceiver system on a single chip using a standard 0.13µm CMOS SOI is described. The system achieves 40Gb/s aggregate data rate on one fiber.

Figure 2.1.1 shows the architecture of the 4-channel DWDM transceiver. In each transmitter channel, a continuous-wave (CW) laser is coupled into an on-chip waveguide using a normal to surface holographic lens (HL) [1]. The HL serves as an "optical pad" designed to couple light in and out of the silicon chip. Each optical channel operates at a different wavelength in the C-band. The wavelength spacing between channels is 200GHz. Each wavelength is modulated in OOK format using electrical data that is amplified by an on-chip modulator driver. The output of the driver provides a nominal 5V differential swing to a high-speed optical modulator also integrated within the same silicon [1]. The high-speed modulator uses a free-carrier effect based device in a Mach-Zehnder interferometer (MZI). The modulated output of the 4 MZIs are combined into a single optical waveguide using a 200GHz-spaced, 4-channel interleaver optical multiplexer. The multiplexed optical signal is coupled out of the chip using another HL.

The receiver signal path begins with an HL that couples the received optical data containing all 4 wavelengths from single-mode fiber into the chip. An optical waveguide steers the light to an interleaver optical demultiplexer that separates the optical signal into its 4 constituent wavelengths with a transfer function identical to the multiplexer interleaver. Each output of the interleaver demultiplexer is guided to a high-speed PIN photodetector (PD) that is flip-chip mounted on the die. Light is coupled from the waveguide into each PD using HL. The PD is mounted on the die in the immediate vicinity of a TIA. A following limiting amplifier (LA) further amplifies the electrical signal.

The optical interleaver is the key element that enables the integration of the optoelectronic DWDM system. It consists of cascaded unbalanced optical interferometric stages that are electrically tunable to achieve any desired wavelength plan. Interleaver multiplexers allow for low-insertion loss combination of the 4 optical wavelengths into one optical waveguide. Interleaver tuning is accomplished by modifying the phase of light propagating in the device using heat created by resistive heaters in the silicon, that were introduced as thermal phase modulators in [4, 5]. Measured channel pass-band spacings in a tuned interleaver optical multiplexer are 1.6nm (200GHz) with an adjacent-channel crosstalk suppression of over 20dB. The demultiplexer interleaver acts identically but in the opposite direction, resulting in demultiplexing the 4 wavelengths to 4 waveguides. Figure 2.1.2 shows the *optical* spectrum at the output of the transmitter. As can be seen all 4 wavelengths are propagating down the same single-mode fiber.

Figure 2.1.3 illustrates the schematic of the modulator driver circuit [4]. It consists of a 3-stage predriver that operates from a 1.5V supply followed by a cascoded differential output driver from a 5V supply. The output stage drives the 50Ω MZI transmission lines with 50Ω far-end terminations. The main challenge in designing the driver is to achieve high voltage swing for the modulator driver while achieving high-speed operation using thin oxide 0.13µm transistors. Therefore, a 5V supply is used to enable large swing while a cascoded thick-oxide transistor is used to protect the switching transistors from over-voltage conditions. The thick-oxide devices also feature a longer channel and can withstand much higher gate and drain-to-source voltages. Inductive peaking is used in the output stage as well as the predriver to achieve fast transitions. Each driver consumes 575mW in nominal conditions. The single-ended input signal can be as low as $50mV_{pk\text{-}pk}$ that will result in an optical output with extinction ratio of about 4dB.

The receiver front-end is shown in Fig. 2.1.4. It consists of a high-speed PIN PD connected to a TIA followed by a 5-stage LA. The PD is flip-chip bonded to the chip. The TIA input stage is based on the resistive feedback structure that achieves low input impedance for high-speed operation. In addition, broadband matching inductors are used in series at the input and in the feedback path. The third stage converts the single-ended input to a differential signal. The second input of this differential amplifier is connected to a replica of the first 2 TIA stages to convert the TIA to pseudo-differential architecture for minimizing crosstalk. The input node of this reference branch is terminated via a dummy capacitor C_{PD}, which matches the junction capacitance of the PD. The limiting amplifier consists of resistively-loaded differential stages with inductive peaking. The output of the LA is filtered to extract the DC-level information of the signal, which is utilized in an offset-cancellation loop. This loop also compensates for the non-zero average input caused by non-ideal extinction ratio of the optical input. The LA drives a 50Ω output buffer. Each receiver operates from a single 1.5V supply. The PD is reverse biased using an integrated low-drop regulator that regulates the 5V supply. The total power consumption is 120mW including the output buffer.

Figure 2.1.5 shows an example optical eye diagram from one transmitter. The TIA in each channel achieves an optical sensitivity of better than -15dBm average power for $BER=10^{-12}$ at 10Gb/s. To test the full optoelectronic operation, the DWDM optical output is externally looped back to the DWDM receiver input. All the 4 channels are operating simultaneously each at 10Gb/s with uncorrelated data applied to all the 4 transmitter inputs. One receiver output is examined and error-free operation is observed when measured overnight ($BER<10^{-14}$). The measured optical power penalty caused by optoelectronic crosstalk between channels is 0.6dB in this test. The bathtub curve of the receiver output is shown in Fig. 2.1.6 that demonstrates the eye opening. The die micrograph with highlighted functions is illustrated in Fig. 2.1.7.

References:

[1] A. Huang, C. Gunn, L. Guo-Liang, et al., "A 10Gb/s Photonic Modulator and WDM MUX/DEMUX Integrated with Electronics in 0.13µm SOI CMOS," *ISSCC Dig. Tech. Papers*, pp.244-245, Feb., 2006.

[2] J.W. Goodman, F.J. Leonberger, S.-Y. Kung, R.A. Athale, "Optical Interconnections for VLSI Systems," *Proc. of the IEEE*, vol. 72, pp.850-866, July, 1984.

[3] D.A.B. Miller, "Rationale and Challenges for Optical Interconnects to Electronics Chips," *Proc. of the IEEE*, vol. 88, pp. 728-749, Jun., 2000.

[4] B. Analui, D. Guckenberger, D. Kucharski, A. Narasimha, "A Fully Integrated 20-Gb/s Optoelectronic Transceiver Implemented in a Standard 0.13µm CMOS SOI Technology," *IEEE J. Solid-State Circuits,* Dec., 2006.

[5] G.T. Reed and A.P. Knights, Silicon Photonics: an Introduction, John Wiley and Sons, 2004, Chapter 4.

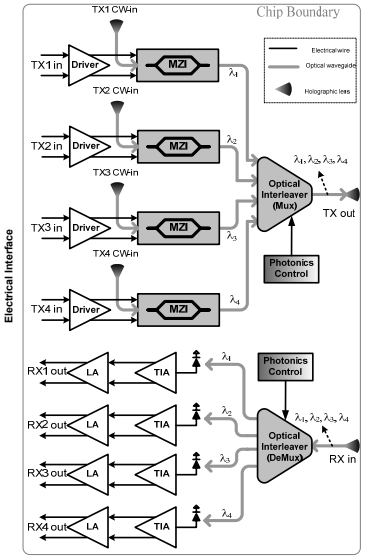

Figure 2.1.1: 4-channel DWDM system architecture.

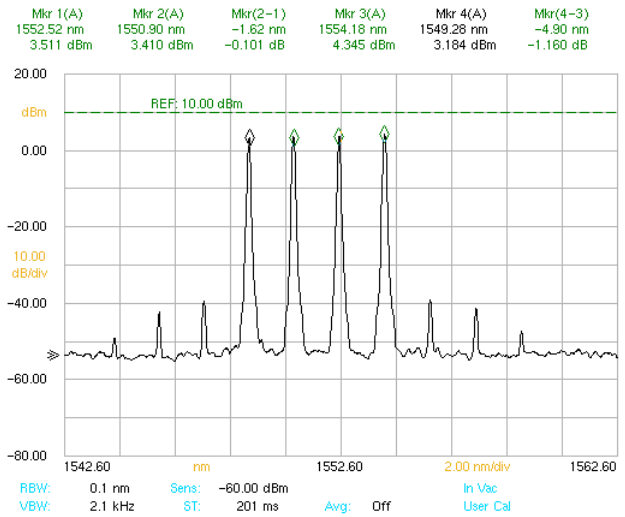

Figure 2.1.2: Measured optical spectrum of the transmitter output.

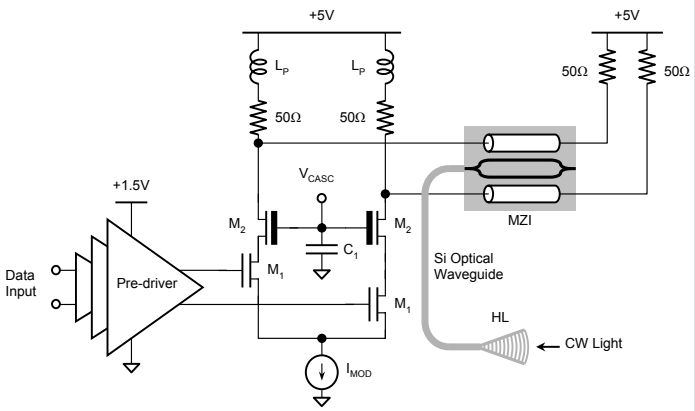

Figure 2.1.3: Modulator driver with Mach-Zehnder interferometer (MZI).

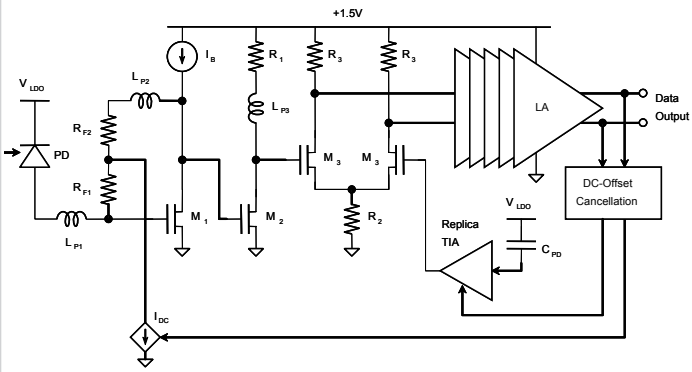

Figure 2.1.4: Simplified schematic of the TIA and limiting amplifier (LA).

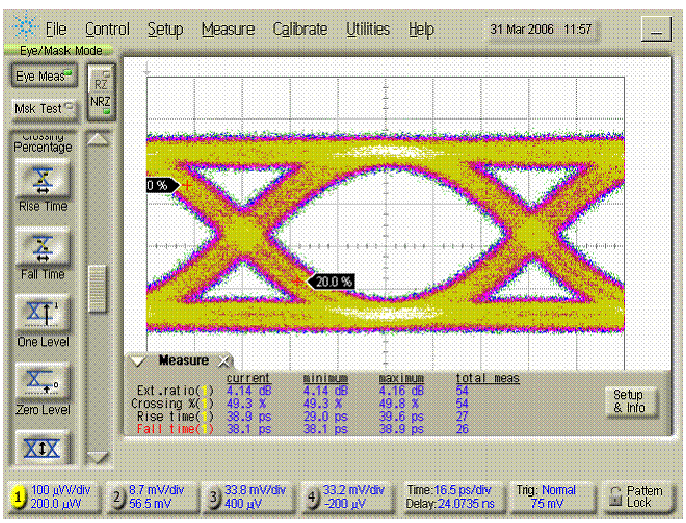

Figure 2.1.5: Transmitter optical output.

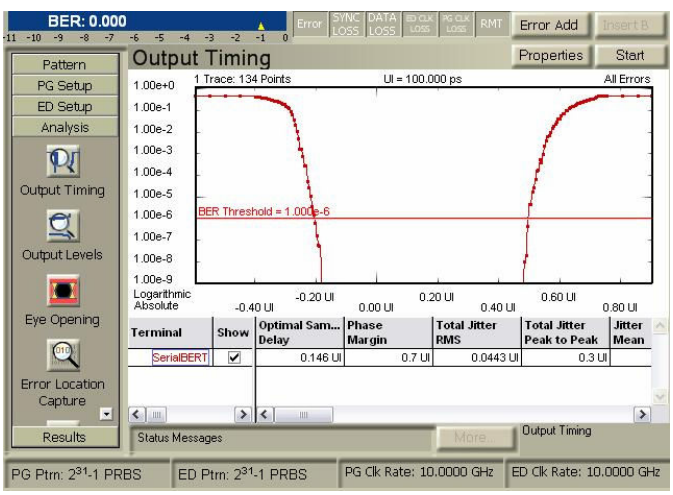

Figure 2.1.6: Receiver bathtub curve with TX1-RX4 external optical loopback.

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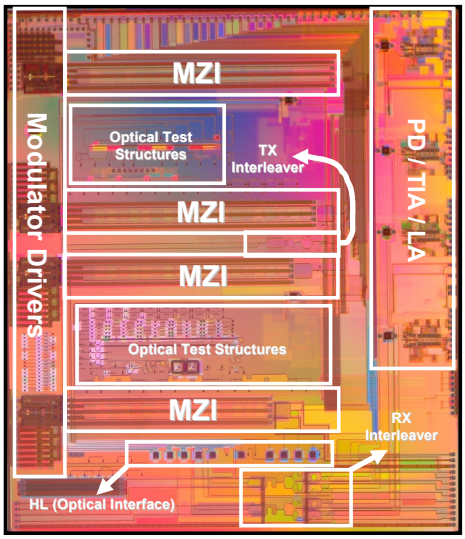

Figure 2.1.7: Die micrograph.

